PLL simulation

Prepared by: Qian Wang
willwq@wpi.edu
Spinlab,Worcester Polytechnic Institute

Version 1.0

October 12, 2006

Abstract

This is a report for Phase-Locked Loop simulation.

Contents

1 Introduction

The PLL is a circuit synchronizing an output signal with a reference or input signal in frequency as well as in phase, in the synchronized state the phase error between the oscillator's output signal and the reference signal is zero, or remains constant.

If a phase error builds up, a control mechanism acts on the oscillator in such a way that the phase error is again reduced to a minimum. In such a control system the phase of the output signal is actually locked to the phase of the reference signal.

This document will deal with the simulaiton of the PLL from the unlocked state to locked state.It is desired to be able to predict the behaviour of the PLL in terms of settling time and locking to specified frequencies. Though the operating principle of the system can be well explained by the example of the linear PLL, in our simulation we want to study the nolinear case.

1.1 System Model

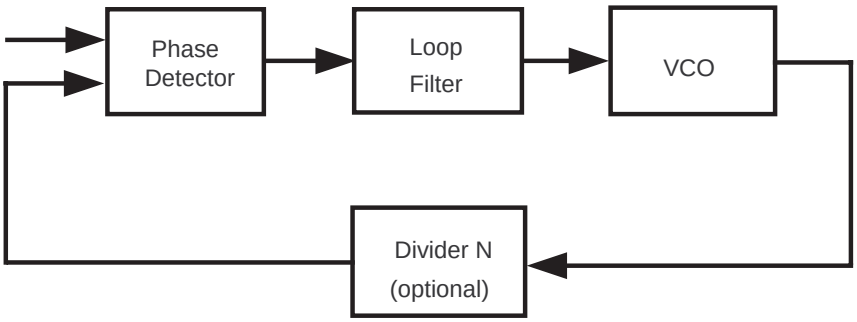


Figure 1: PLL system model

The PLL block diagram is shown in Fig.1. It consists of three basic functional blocks:

- Phase Detector (PD)
- Loop Filter (LF)
- Voltage Controlled Oscillator (VCO)

In our simulation, we will take a look at its behavior in the unlocked state of the PLL. when the PLL is out of lock, the frequency between input signal and output signal are different. The higher harmonics are suppressed by the loop filer, there remains one AC term. Consequently there will be a nonzero DC component that will pull the average output frequency of the VCO up or down until lock is acquired.The signals of interest within the PLL circuit are defined as follows:

1. The input signal $u_1(t)$
2. The angular frequency ω_1 of the input signal
3. The output signal $u_2(t)$ of the VCO

4. The angular frequency ω_2 of the output signal
5. The output signal $u_d(t)$ of the phase detector
6. The output signal $u_f(t)$ of the loop filter
7. The phase error θ_e, defined as the phase difference between signals $u_1(t)$ and $u_2(t)$

phase detector is a circuit capable of delivering an output signal $u_d(t)$ that is approximately proportional to the phase difference between the output signal and the feedback signal. There are mainly four types of phase detectors are used. In our simulation will compare the characteristics of multiplier and EXOR.

- Multiplier phase detector. We use sine wave as the input signal and the feedback signal. The output signal of the multiplier is obtained by multiplying the two signals. when the PLL is locked, the frequences ω_1 and ω_2 are identical.
- EXOR phase detector. The operation of the EXOR phase is similar to that of the multiplier. We also assume that both the input and the feedback signal are sine waves.

A loop filter is a lowpass filter, it filters out the higer frequencies and pass the lower ones. After the PD develop a nonzero output, the LF would aslo produce a finite signal $u_f(t)$. In our simulation, we will use second-order active PI filter.

The VCO oscillates at an angular frequency ω_2, which is determined by the output signal $u_f(t)$. With time elapsing, VCO will increase its frequency. when settled, VCO will operates at frequency greater than its center frequency ω_0 by $\Delta\omega$. At this time, $u_f(t)$ will settle at a final value of $\frac{\Delta\omega}{K_0}$.

2 Matlab Analysis

2.1 Parameters Specification

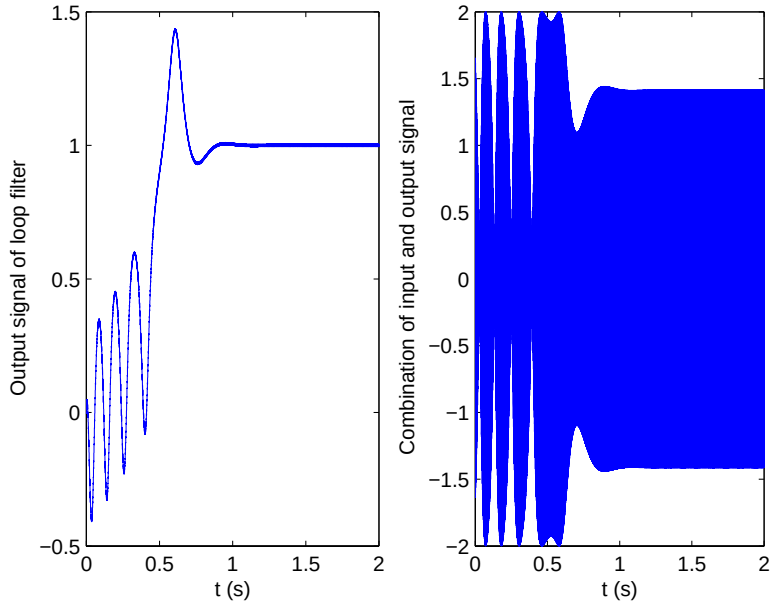
The simulation parameters are as below:

- $f_s = 44.1e^3$
- $K_0 = 20\pi$
- $K_d = 1$

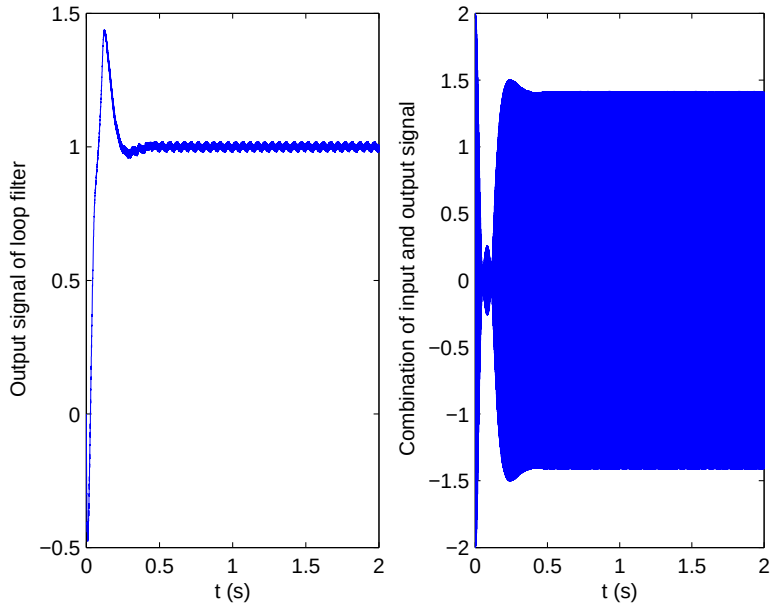
2.2 Phase Detector: Multiplier and EXOR

We can use Matlab to compare the performance of the system using these two different phase detectors, the characteristics of the system are shown below.

1. Multiplier phase detector, ω_0=$2\pi e^3$, $\Delta\omega$=20π.



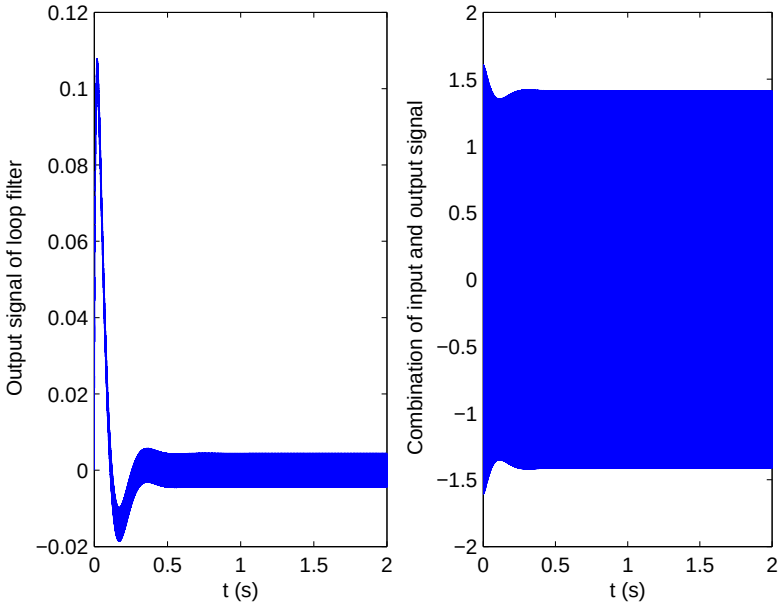
2. EXOR phase detector, ω_0=$2\pi e^3$, $\Delta\omega$=20π.



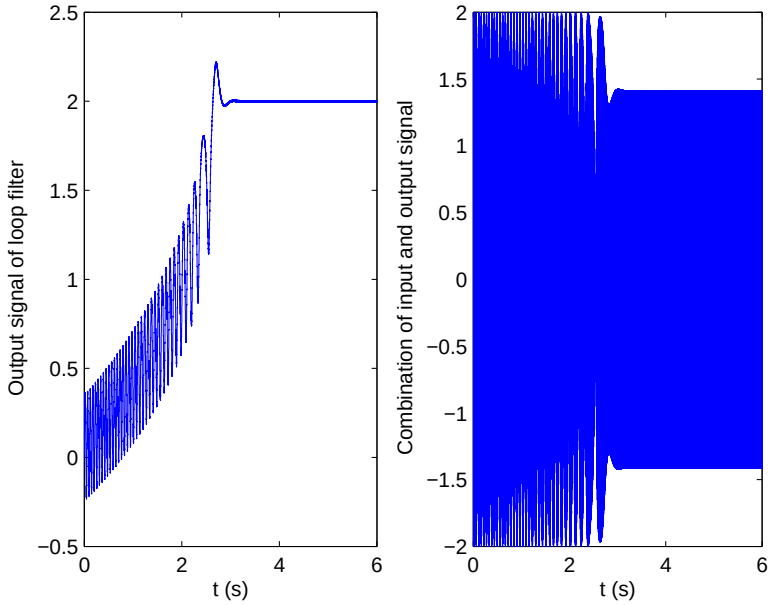
We can see that by using EXOR phase detector the system settles more quickly. There are some ripples occurring during the settled period when EXOR is employed. Actually, these are square waves caused by XOR function.

2.3 VCO Center Frequency and Input Signal Frequency

1. $\Delta\omega$=$\omega_0 - \omega_1 = 0$, ω_0=$2\pi e^3$, PD type=Multiplier.



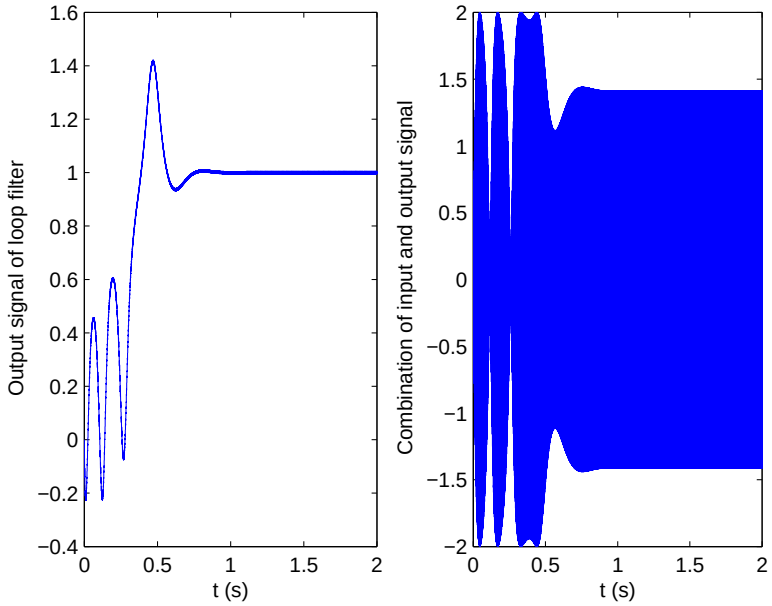
2. $\Delta\omega$=$\omega_0 - \omega_1 = 40\pi$, ω_0=$2\pi e^3$, PD type=Multiplier.



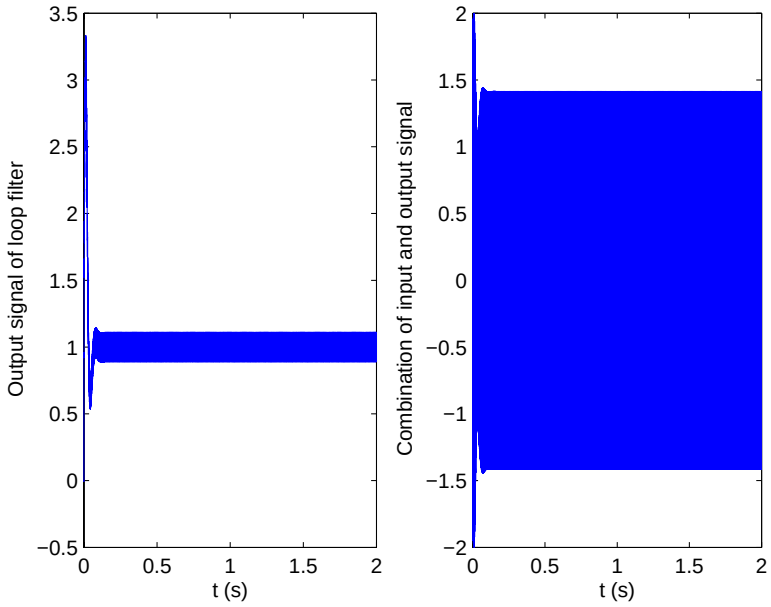
We can see from the plots that if input frequency and the VCO center frequency are the same at the initial start, it needs the least time to get settled and the $u_f(t)$ is at a final value of zero.

2.4 Bandwidth of PLL ω_{3dB}

1. ω_{3dB}=$0.01\omega_0$, $\Delta\omega$=20π, ω_0=$2\pi e^3$, PD type=Multiplier.



2. ω_{3dB}=0.05ω_0, $\Delta\omega$=20π, ω_0=2πe^3, PD type=Multiplier.



We can see that when utilizing larger bandwith, the system can tracks phase and frequency variations of the input signal more rapidly. But at the same time, high frequency components and noise can not be well supressed.

3 Conclusion

References

[1] R.E.Best, *Phase-Locked Loops: Design, Simulation, and Applications*, McGraw-Hill, New York,2003.

[2] P.Z.Peebles, *Probability,Random Variables,and Random Signal Principles*, McGraw-Hill, New York,1993.