EE230x Hw#3 Solutions

8.12 The capacity of the T1 line is 1.544 Mbps. The available capacity is 1.544 ·0.99 =1.52856 Mbps = AC.
a. AC/110 = 13,896
b. AC/300 = 5,095
c. AC/1200 = 1273
d. AC/9600 = 159
e. AC/64000 = 23
If the sources were active only 10% of the time, a statistical multiplexer could be used to boost the number of devices by a factor of about seven or eight in each case. This is a practical limit based on the performance characteristics of a statistical multiplexer.

8.13 Synchronous TDM: 9600 bps · 10 = 96 kbps
Statistical TDM: 9600 bps ·10· 0.5/0.8 = 60 kbps

10.4 The argument ignores the overhead of the initial circuit setup and the circuit teardown.

10.5
a. Circuit Switching
$T = C_1 + C_2$ where
C_1 = Call Setup Time
C_2 = Message Delivery Time
$C_1 = S = 0.2$
C_2 = Propagation Delay + Transmission Time
$= N \cdot D + L/B$
$= 4 \cdot 0.001 + 3200/9600 = 0.337$
$T = 0.2 + 0.337 = 0.537$ sec

Datagram Packet Switching
$T = D_1 + D_2 + D_3 + D_4$ where
D_1 = Time to Transmit and Deliver all packets through first hop
D_2 = Time to Deliver last packet across second hop
D_3 = Time to Deliver last packet across third hop
D_4 = Time to Deliver last packet across forth hop
There are $P – H = 1024 – 16 = 1008$ data bits per packet.
A message of 3200 bits requires four packets
(3200 bits/1008 bits/packet = 3.17 packets which we round up to 4 packets).
$D_1 = 4 \cdot t + p$ where
t = transmission time for one packet
p = propagation delay for one hop
$D_1 = 4 \cdot (P/B) + D$
$= 4 \cdot (1024/9600) + 0.001$

$= 0.428$

$D_2 = D_3 = D_4 = t + p$

$= (P/B) + D$

$= (1024/9600) + 0.001 = 0.108$

$T = 0.428 + 0.108 + 0.108 + 0.108$

$= 0.752$ sec

Virtual Circuit Packet Switching

$T = V_1 + V_2$ where

V_1 = Call Setup Time

V_2 = Datagram Packet Switching Time

$T = S + 0.752 = 0.2 + 0.752 = 0.952$ sec

b. Circuit Switching vs. Diagram Packet Switching

T_c = End-to-End Delay, Circuit Switching

$T_c = S + N \cdot D + L/B$

T_d = End-to-End Delay, Datagram Packet Switching

N_p = Number of packets $= \left\lceil \frac{L}{P-H} \right\rceil$

$T_d = D_1 + (N - 1)D_2$

D_1 = Time to Transmit and Deliver all packets through first hop

D_2 = Time to Deliver last packet through a hop

$D_1 = Np(P/B) + D$

$D_2 = P/B + D$

$T = (N_p + N - 1)(P/B) + N \times D$

$T = T_d$

$S + L/B = (N_p + N - 1)(P/B)$

Circuit Switching vs. Virtual Circuit Packet Switching

T_V = End-to-End Delay, Virtual Circuit Packet Switching

$T_V = S + T_d$

$T_C = T_V$

$L/B = (Np + N - 1)(P/B)$

Datagram vs. Virtual Circuit Packet Switching

$Td = TV - S$

10.11

$$k = 2 + 2 \cdot \frac{T_{td} \times R_u}{8 \times L_d}$$

$$= 2 + 2a$$

Where the variable *a* is the same one defined in Chapter 7. In essence, the upper part of the fraction is the length of the link in bits, and the lower part of the fraction is the length of a frame in bits. So the fraction tells you how many frames can be laid out on the link at one time. Multiplying by 2 gives you the round-trip length of the link. You want your sliding window to accommodate that number of frames so that you can continue to send frames until an acknowledgment is received. Adding 1 to that total takes care of rounding up to the next whole number of frames. Adding 2 instead of 1 is just an additional margin of safety.

See Figure 7.11.