

ECE4703 Midterm Exam

Your Name: SOLUTION Your box #: _____

November 21, 2013

Tips:

- Look over all of the questions before starting.
- Budget your time to allow yourself enough time to work on each question.
- Write neatly and show your work! Points may be deducted for a disorderly presentation of your solution.
- This exam is worth a total of 200 points.
- Attach your “cheat sheet” to the exam when you hand it in.

problem 1	problem 2	problem 3	problem 4	total midterm exam score
45 points	50 points	50 points	55 points	200 points

1. 45 points total. The following questions are with regards to the specific behavior of the ADC/DAC on the TMS320C6713 DSK.

- (a) 15 points. Suppose the sampling frequency on the TMS320C6713 DSK is 44.1 kHz and you have a sinusoidal analog input signal to the ADC given as $x(t) = a \cos(2\pi ft)$ with $a = 2$ volts and $f = 30$ kHz. What happens?

$$30 \text{ kHz} > \frac{f_s}{2} = 22.05 \text{ kHz}$$

The DSK does not allow aliasing and will block this 30 kHz signal with an anti-aliasing filter. The samples will be approximately zero.

- (b) 15 points. What DSK sampling frequencies could you use if you wished to process an analog signal $x(t) = a \cos(2\pi ft)$ with $a = 2$ volts and $f = 21$ kHz?

Possible DSK sampling frequencies:

$$8 \text{ kHz}, 16 \text{ kHz}, 32 \text{ kHz}, 44.1 \text{ kHz}, 48 \text{ kHz}, 96 \text{ kHz}$$

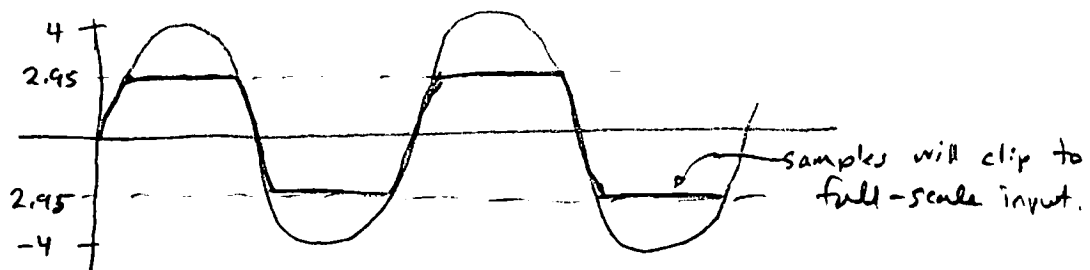
these will block the signal at $f = 21 \text{ kHz}$

these will work, although the anti-aliasing filter may partially block the 21 kHz input when $f_s = 44.1 \text{ kHz}$

- (c) 15 points. Now suppose the sampling frequency on the TMS320C6713 DSK is 44.1 kHz and you have a sinusoidal analog input signal to the ADC given as $x(t) = a \cos(2\pi ft)$ with $a = 4$ volts and $f = 10$ kHz. What happens?

The full-scale input voltage on the ADC is $\approx 5.9 \text{ V}_{pp}$.

When $a = 4 \text{ V}$, we have $V_{pp} = 8$. The signal is not blocked by the anti-aliasing filter but is clipped



2. 50 points total. Recall that the TMS320C6713 DSK is clocked at 225 MHz. Suppose you implement the following guitar effects in C using floating point arithmetic and profile each effect with the following results.

Effect	Cycles to Execute Effect
Distortion	1500
Compressor	2000
Chorus	3000
Flanger	3500
Phase	5000
Ring Modulator	5500

- (a) 20 points. Which of these effects will run in real-time if the sampling frequency is $f_s = 96$ kHz? Explain.

$$\text{Maximum processing time} = \frac{1}{96\text{kHz}} = 10.42\mu\text{s}$$

$$(10.42\mu\text{s})(225\text{ cycles/sec}) \approx 2343\text{ cycles (maximum)}$$

Hence, only the distortion and compressor effects can run in real time.

- (b) 30 points. What could you do to get *all* of the effects to run in real time? Be specific and discuss any tradeoffs in your choices.

Since this is an audio processor there isn't much benefit to using $f_s = 96$ kHz.

1. Lower the sampling frequency to 44.1 kHz

⇒ This gives ≈ 5100 cycles to do the processing which makes all the effects run in real time except ring modulator.

2. To get the last effect to run in real time, we could

a) Try the optimizing compiler

b) Switch to fixed-point arithmetic

c) Try hand-optimizing critical parts of the code in ASM.

At least one of those should work. If not, we could lower the sampling frequency to 32 kHz, but some fidelity would be lost. 3

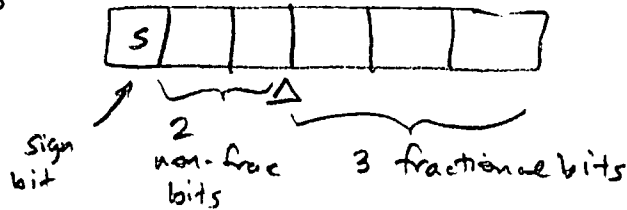
3. 50 points total. You are given the following infinite-precision FIR filter coefficients.

$$b = [\pi \quad -\sqrt{2} \quad e]$$

- (a) 20 points. Suppose you are required to store these filter coefficients in a signed 6-bit fixed-point data type. Determine the optimum number of fractional bits to use in your fixed-point representation of the filter coefficients. Show your reasoning.

π is the largest coefficient, requiring two non-fractional bits.

so



is the best choice to use the most bits.

(Q-3)

- (b) 30 points. Using your fractional bit specification from part (a), fill out the following table. Use the symbol Δ to show the binary decimal point and recall that negative numbers are represented by two's complement.

Coefficient Value	Quantized Value (decimal)	Quantized value (binary)	Quantization Error
π	3.125	$011_{\Delta}001$	$\approx 16.6 \times 10^{-3}$
$-\sqrt{2}$	-1.375	$110_{\Delta}101$	$\approx 39.2 \times 10^{-3}$
e	2.750	$010_{\Delta}110$	$\approx 31.7 \times 10^{-3}$

$\sqrt{2} \approx 1.414$ best quantized value is $1.375 = 001_{\Delta}011$

two's complement :

$$\begin{array}{r} 110100 \\ + 000001 \\ \hline 110101 \end{array}$$

$e \approx 2.718$ best quantized value is $2.75 = 010_{\Delta}110$

4. 55 points. Suppose all quantities in the IIR direct form II system shown in Figure 1 are 16-bit fixed point. Further suppose:

- the feedback coefficients a_1, a_2 are $Q - 15$ shorts
- the feedforward coefficients b_0, b_1, b_2 are $Q - 18$ shorts
- the intermediate results $u[n], u[n - 1], u[n - 2]$ are all $Q - 12$ shorts.

Determine all of the shifts necessary to correctly perform the calculations and avoid overflow at any point in the processing. Explain your choices. Clearly annotate the figure below with your "shift plan".

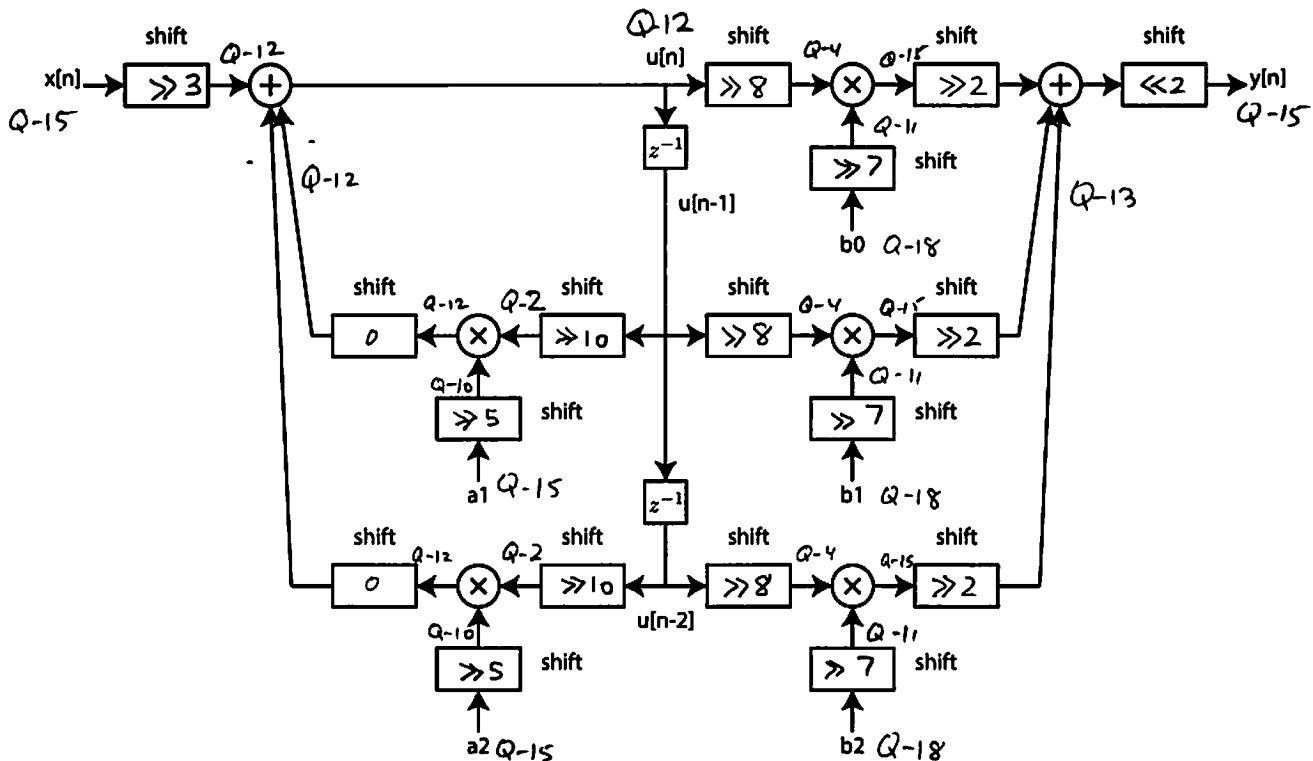


Figure 1: Fixed-point direct form II IIR filter.

Products: Need to throw away a total of 15 bits to guarantee no overflow.

- On the feedback side, I went with 10/5 for the intermediate values / coefficients to preserve detail in the coefficients
- on the feedforward side, I went with 8/7 since the b coefficients are less sensitive.

Sums: The feedback sum required no shifts to align with $Q-12$.
The feedforward sums have two-bit shifts to avoid overflow.

Other: The input is shifted by 3 bits to align with a $Q-12$ sum.
The final two-bit left shift puts the output in $Q-15$ format.